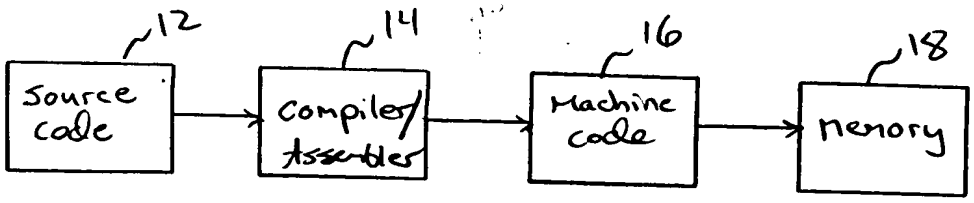


Fig. 1

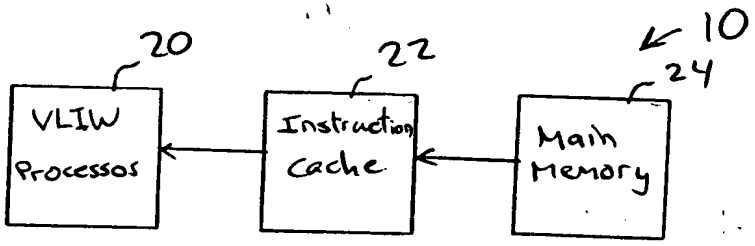


Fig. 2

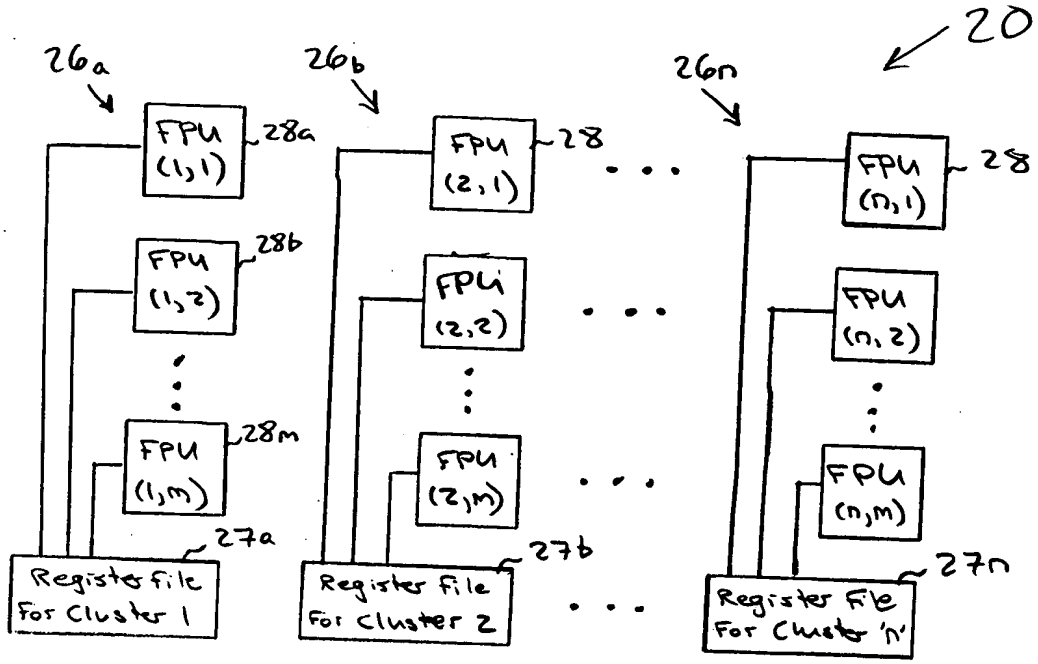


Fig. 3

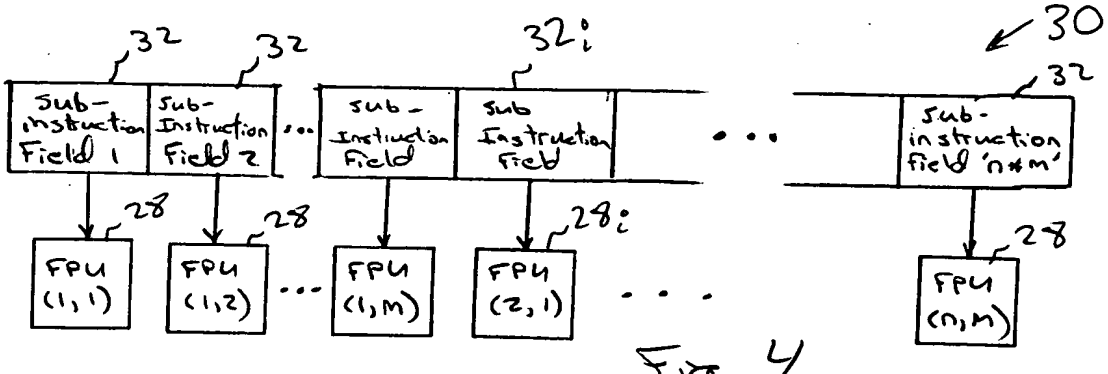


Fig. 4

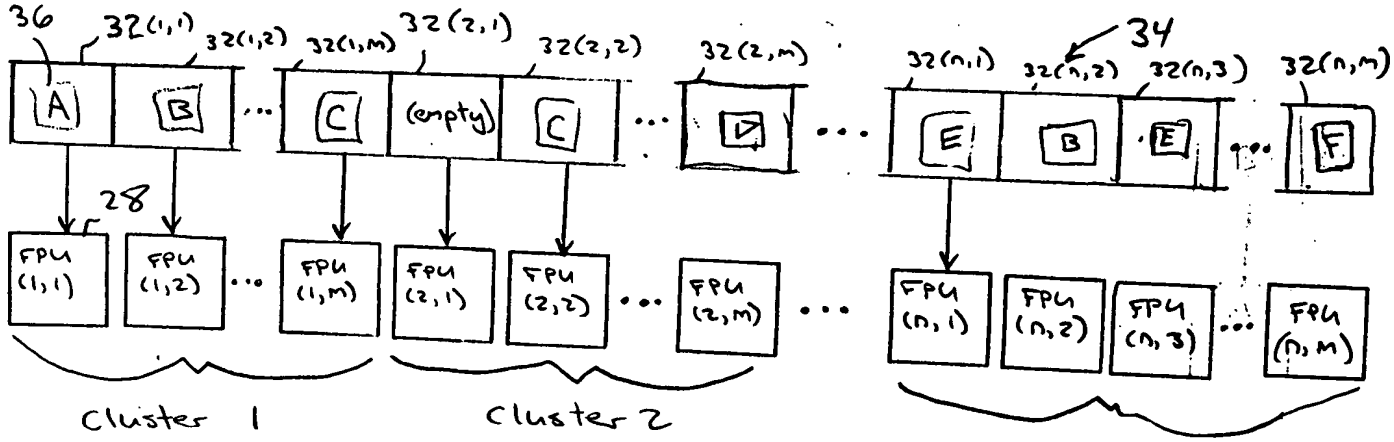


Fig. 5

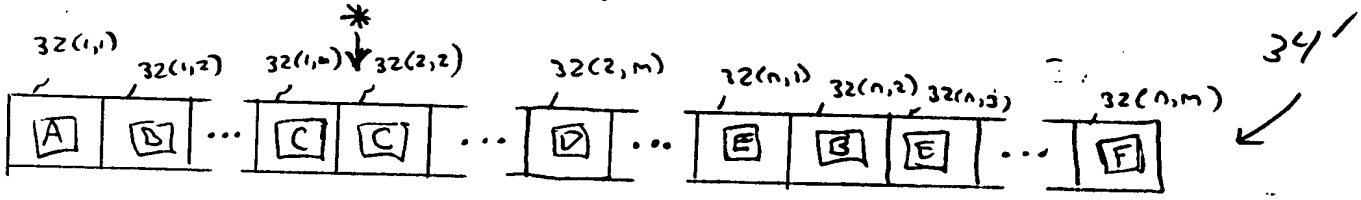


Fig. 6

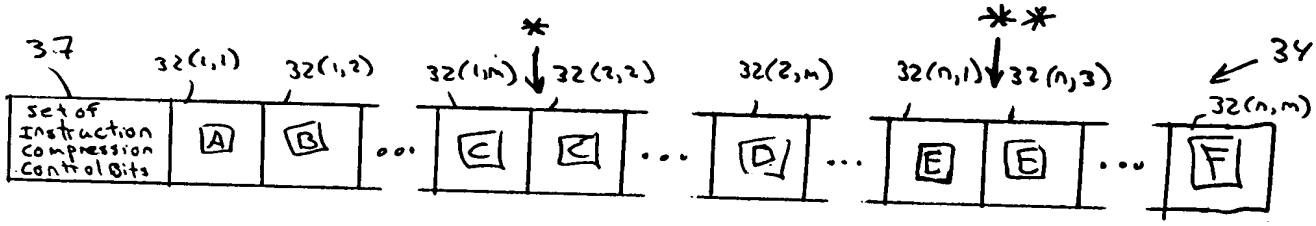


Fig. 7

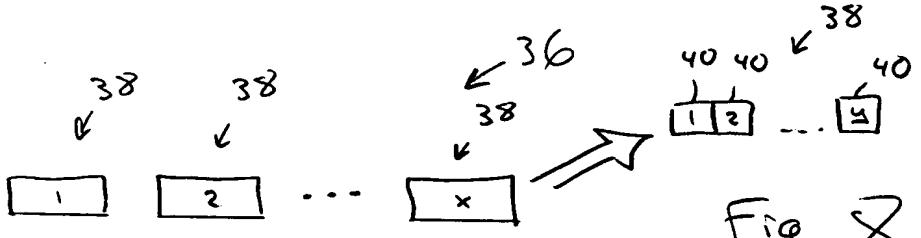


Fig. 8

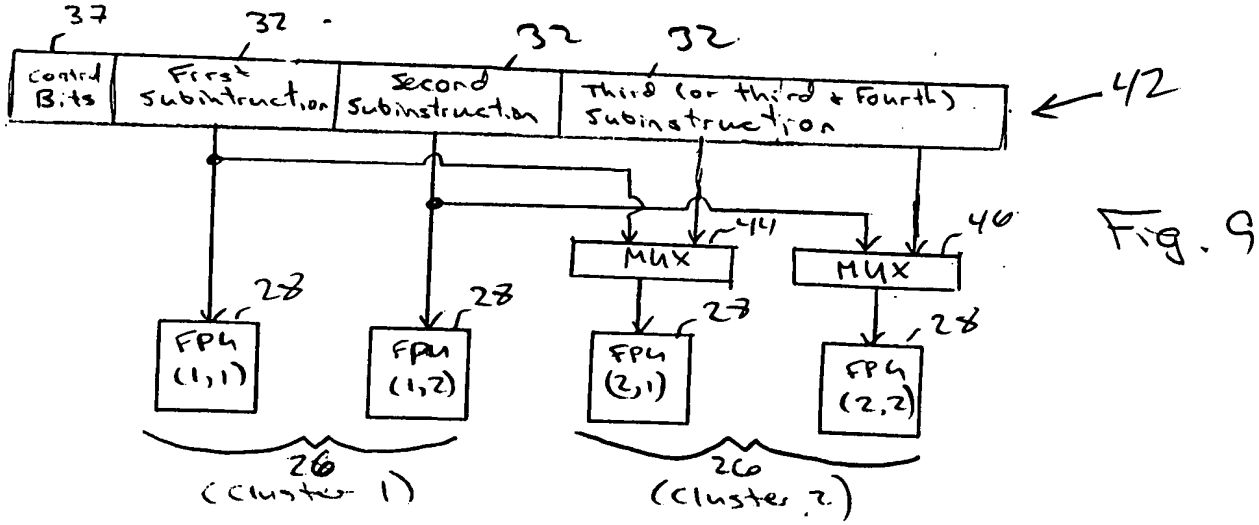
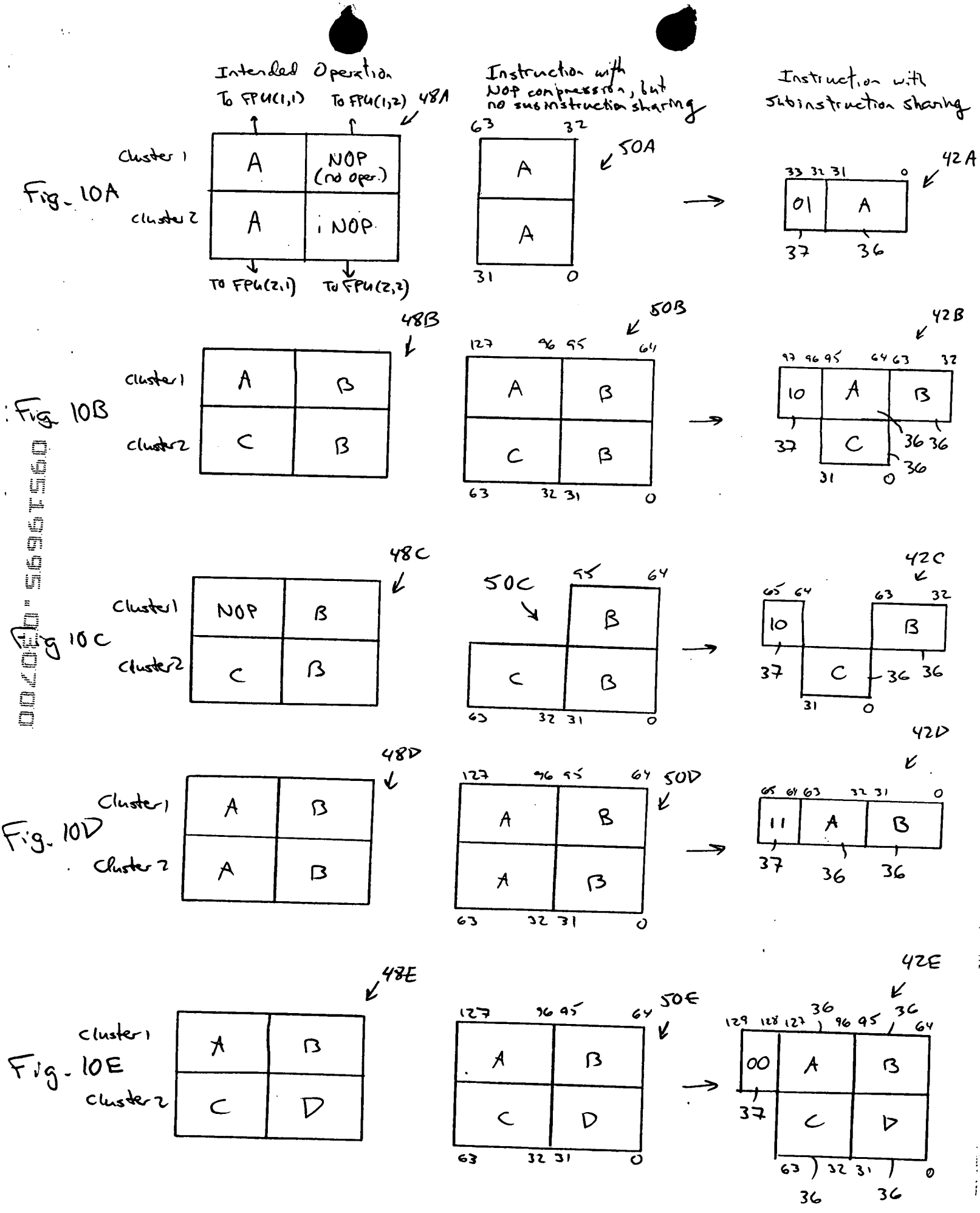


Fig. 9


Intended Operation
To FPU(1,1)
To FPU(1,2)
48A
Cluster 1
Cluster 2
A
NOP (no oper.)
A
NOP
To FPU(2,1)
To FPU(2,2)
Fig. 10A
Instruction with NOP compression, but no subinstruction sharing
63
32
A
A
50A
31
0
Instruction with subinstruction sharing
42A
33 32 31
0
01
A
37
36
48B
Cluster 1
Cluster 2
A
B
C
B
Fig. 10B
50B
127
96 95
64
A
B
C
B
63
32 31
0
42B
97 96 95
64 63
32
10
A
B
C
37
36 36
36
31
0
48C
Cluster 1
Cluster 2
NOP
B
C
B
Fig. 10C
50C
95
64
B
C
B
63
32 31
0
42C
65 64
63
32
10
B
C
37
36 36
31
0
48D
Cluster 1
Cluster 2
A
B
A
B
Fig. 10D
127
96 95
64
50D
A
B
A
B
63
32 31
0
42D
65 64 63
32 31
0
11
A
B
37
36
36
48E
Cluster 1
Cluster 2
A
B
C
D
Fig. 10E
127
96 95
64
50E
A
B
C
D
63
32 31
0
42E
36
36
129 128 127
96 95
64
00
A
B
37
C
D
63
32 31
0
36
36

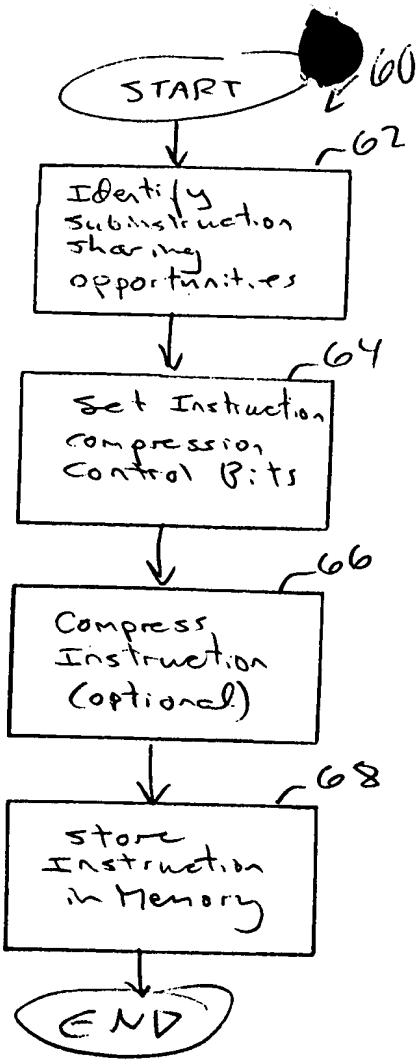


Fig. 11

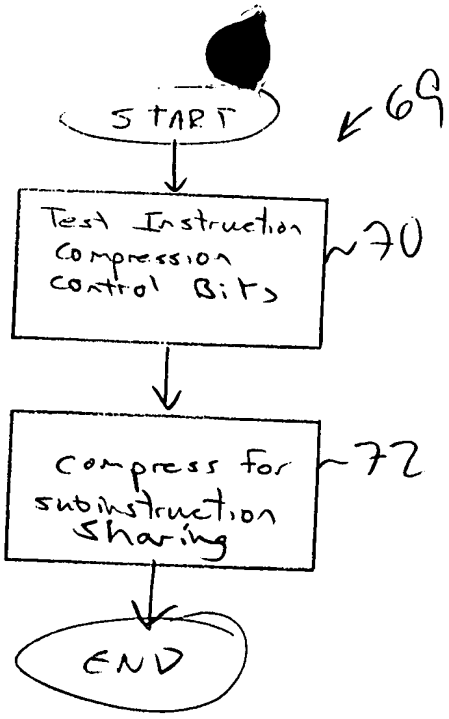


Fig. 12

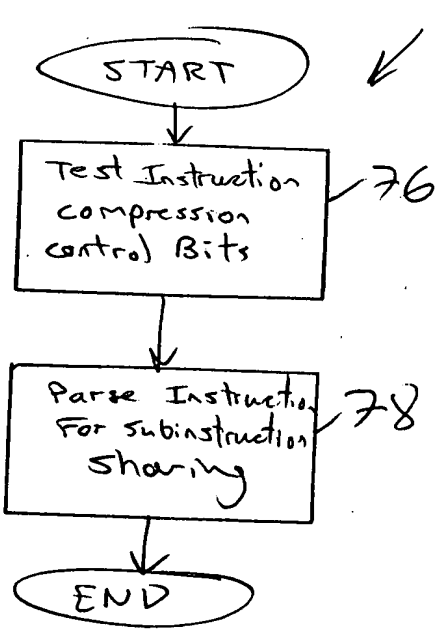


Fig. 13

09570360.050501